

REMARKS/ARGUMENTS

The Applicant originally submitted Claims 1-20 in the application. In the present response, the Applicant canceled Claims 1-15 without prejudice or disclaimer. No other Claims have been amended, canceled, or added. Accordingly, Claims 16-20 are currently pending in the application.

I. Rejection of Claims 1, 6, and 11 under 35 U.S.C. §102

The Examiner has rejected Claims 1, 6, and 11 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,905,766 to Nguyen. The rejection, however, is now moot since Claims 1, 6, and 11 have been canceled without prejudice or disclaimer. Accordingly, the Applicant respectfully requests the Examiner to withdraw the §102(b) rejection and allow issuance of the pending claims.

II. Rejection of Claims 2-5, 7-10, and 12-15 under 35 U.S.C. §103

The Examiner has rejected Claims 2-5, 7-10, and 12-15 under 35 U.S.C. §103(a) as being unpatentable over Nguyen in view of U.S. Patent No. 6,260,152 by Cole, *et al.* The rejection, however, is now moot since Claims 2-5, 7-10, and 12-15 have been canceled without prejudice or disclaimer. Accordingly, the Applicant respectfully requests the Examiner to withdraw the §103(a) rejection and allow issuance of the pending claims.

III. Rejection of Claims 16-20 under 35 U.S.C. §103

The Examiner has rejected Claims 16-20 under 35 U.S.C. §103(a) as being unpatentable over Nguyen in view of Cole, and in further view of U.S. Patent No. 6,594,327 to Radi. The Applicant respectfully disagrees.

The cited combination of Nguyen, Cole, and Radi, as discussed in the telephonic interview, does not teach or suggest a fast pattern processor comprising an output interface subsystem including a first-in-first-out buffer as recited in independent Claim 16. Nor does the cited combination teach or suggest an event edge synchronization system that provides a synchronous notification signal indicating that a block of data of the FIFO buffer has been retrieved and re-transmitted as recited in independent Claim 16. Additionally it was noted in that the pending rejection did not assert the same.

In the Examiner's Final rejection mailed November 24, 2006, the Examiner asserts that the LAN Interface **104** and the Incoming Data Processing Unit **106** discloses the output interface subsystem of Claim 16. (*See Examiner's Final Rejection mailed November 24, 2006, page 7.*) Even assuming *arguendo* this to be true, as pointed out to the Examiner, neither the LAN Interface **104** nor the Incoming Data Processing Unit **106** contain a FIFO buffer. (*See Figures 1 and 2.*) Additionally, neither the LAN Interface **104** nor the Incoming Data Processing Unit **106** include an event edge synchronization system that provides a synchronous notification signal indicating that a block of data of the FIFO buffer has been retrieved and re-transmitted. Furthermore, the Applicant does not find any other teaching or suggestion in Radi of such an output interface subsystem as recited in independent Claim 16.

As such, the cited combination of Nguyen, Cole, and Raddi does not teach or suggest each element of independent Claim 16 and, therefore, does not provide a *prima facie* case of obviousness for independent Claim 16 and Claims dependent thereon. Accordingly, Claims 16-20 are not unpatentable in view of the cited combination and the Applicant respectfully requests the Examiner to withdraw the §103(a) rejection of Claims 16-20 and allow issuance thereof.


IV. Conclusion

In view of the foregoing amendment and remarks, the Applicant now sees all of the Claims currently pending in this application to be in condition for allowance and therefore earnestly solicits a Notice of Allowance for Claims 16-20.

The Applicant requests the Examiner to telephone the undersigned attorney of record at (972) 480-8800 if such would further or expedite the prosecution of the present application. The Commissioner is hereby authorized to charge any fees, credits or overpayments to Deposit Account 08-2395.

Respectfully submitted,

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